14 – Technology of Vision

Prof Peter YK Cheung

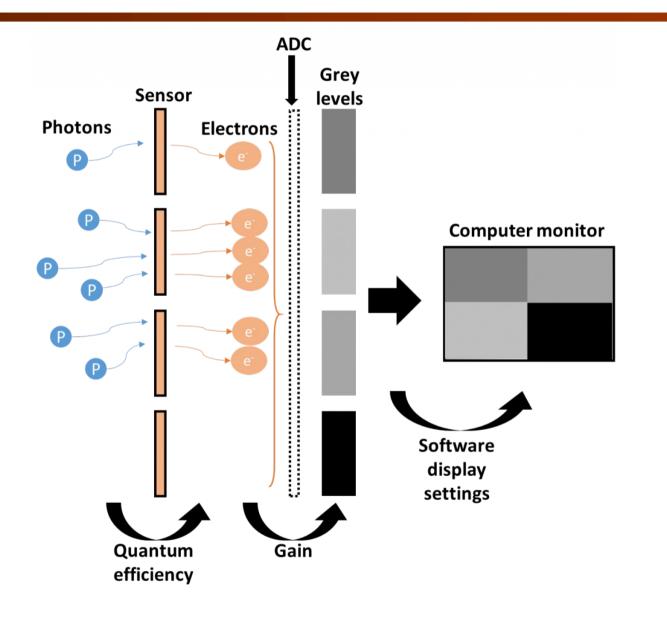
Dyson School of Design Engineering

URL: www.ee.ic.ac.uk/pcheung/teaching/DE4_DVS/ E-mail: p.cheung@imperial.ac.uk

Three Categories of Vision Technology

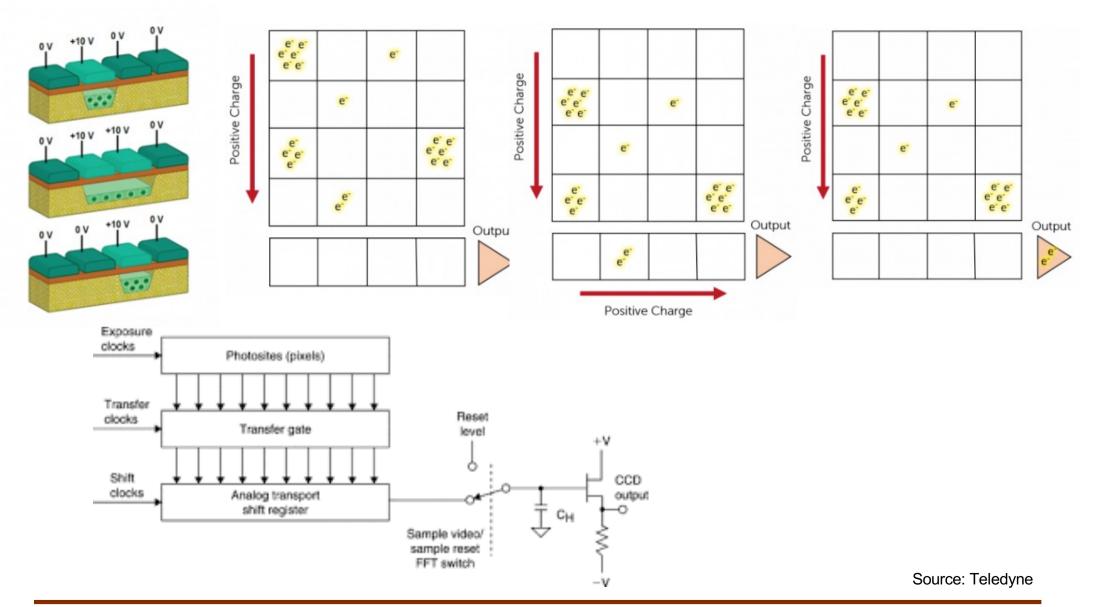
- Sensors for vision
 - Visible light image sensors
 - IR image sensors
 - Time of Flight (ToF) image sensors
- Display Technology
 - Thin-film Transistor (TFT) Liquid Crystal Displays(LCD)
 - In-Plan Switch (IPS) Liquid Crystal Displays (LCD)
 - Organic LED (OLED) Displays
 - Digital Light Processing (DLP) Projectors
- Visual Data Processors
 - Graphics Processing Units (GPU)
 - Al/Neuro Processors

Photons to Electrons



Source: Teledyne

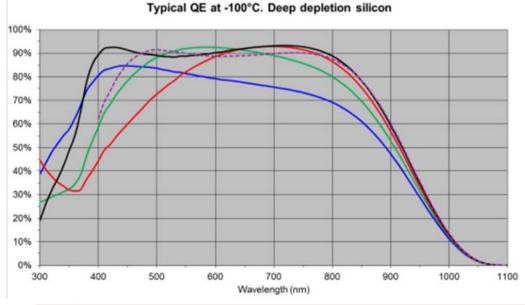
CCD Sensor Technology



Example of a CCD Sensor

Teledyne CCD290-99 Scientific CCD Sensor, 9216 x 9232 Pixels





Number of pixels	er of pixels 9216 (H) × 9232 (V)	
Pixel size	10 µm square	
Image area	92.2 mm × 92.4 mm	
Outputs	16	
Package size	98.5 × 93.7 mm	
Package format	Silicon carbide with two flexi connectors	
Focal plane height, above base	20.0 mm	
Connectors	Two 51-way micro-D	
Flatness	20 µm (peak to valley)	
Amplifier sensitivity	7.5 μV/e⁻	
Read-out noise	4 e [−] at 0.5 MHz 2.5 e [−] at 50 kHz	
Maximum pixel data rate	3 MHz	
Charge storage (pixel full well)	90,000 e [−]	
Dark signal	4 e [−] /pixel/hour (at –100 °C)	
	Source: Teledyne	

Example of a CCD Camera



Specification Maximum Pixel Output CCD Pixel Size (Shape) **CCD Chip Size** CCD Cooling Fastest Shutter Speed Slowest Shutter Speed Sensitivity Setting Exposure Control Signal/Noise Dynamic Range Dark Current Read Noise Well Depth Resolution Live Image **Display Rate** Maximum Image Size **Image Storage Format** Lens Mount **Computer Interface**

Nikon DXM 1200 12 Million Sony ICX085AK (Bayer Mosaic Filters) 6.7 Microns (Square) 10.0 (H) x 8.7 (V) (Millimeters) None 1/12000 Seconds 170 Seconds 3 Levels (Normal, High, Max Manual 50 dB 8 Bits (48 dB) 4 Electrons/Pixel/Second 16 Electrons/Pixel 16,000 Electrons 1800 TV Lines 12 Frames/Second 3840 x 3072 Pixels TIF, BMP, JPG C-mount

PCI BusMaster

Source: Nikon

Sample images from CCD microscope

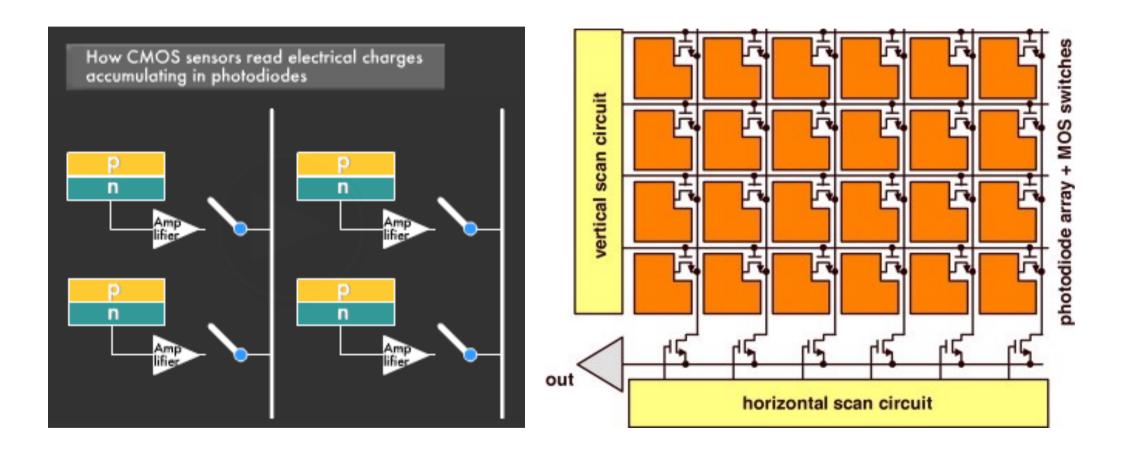


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PYKC 11 March 2025

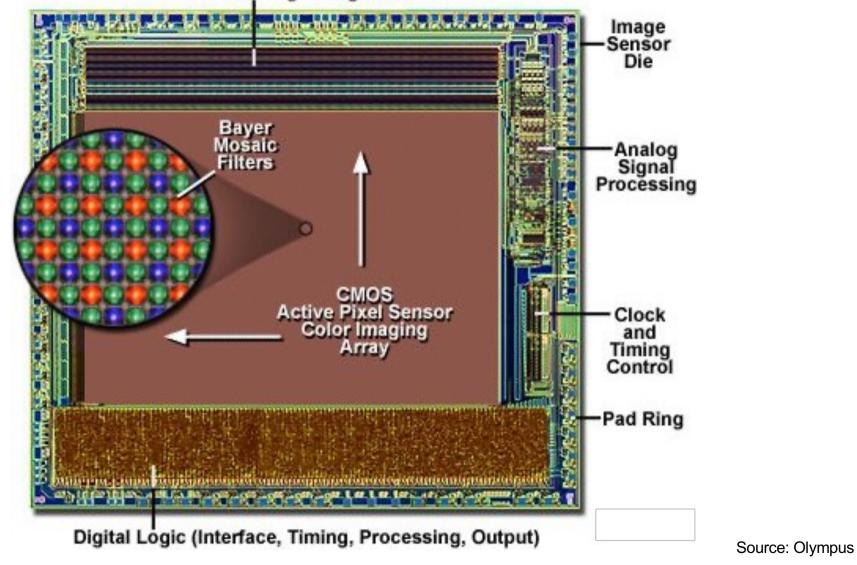
Lecture 14 Slide 7

CMOS Sensor – photodiode array



Structure of a CMOS Sensor Device

Analog-to-Digital Conversion

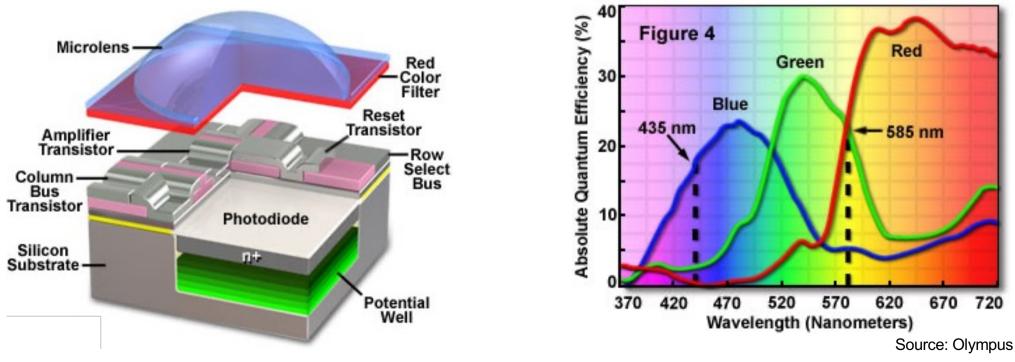


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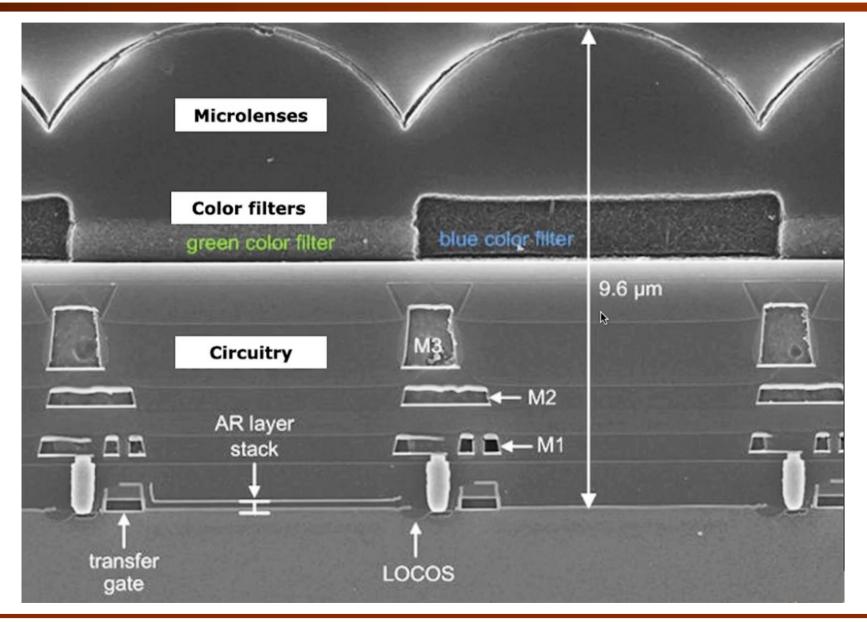
Bayer Mosaic Filter arrangement







SEM image of Cross Section of a CMOS Sensor



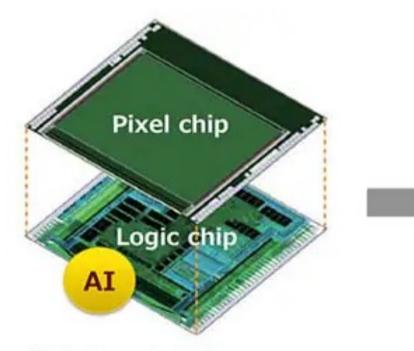
Low Cost Camera - Raspberry Pi

	Camera Module v1	Camera Module v2	Camera Module 3	Camera Module 3 Wide	HQ Camera	GS Camera
Net price	\$25	\$25	\$25	\$35	\$50	\$50
Size	Around 25 × 24 × 9 mm	Around 25 × 24 × 9 mm	Around 25 × 24 × 11.5 mm	Around 25 × 24 × 12.4 mm	38 x 38 x 18.4mm (excluding lens)	38 x 38 x 19.8mm (29.5mm with adaptor and dust cap)
Weight	3g	3g	4g	4g	30.4g	34g (41g with adaptor and dust cap)
Still resolution	5 Megapixels	8 Megapixels	11.9 Megapixels	11.9 Megapixels	12.3 Megapixels	1.58 Megapixels
Video modes	1080p30, 720p60 and 640 × 480p60/90	1080p47, 1640 × 1232p41 and 640 × 480p206	2304 × 1296p56, 2304 × 1296p30 HDR, 1536 × 864p120	2304 × 1296p56, 2304 × 1296p30 HDR, 1536 × 864p120	2028 × 1080p50, 2028 × 1520p40 and 1332 × 990p120	1456 x 1088p60
Sensor	OmniVision OV5647	Sony IMX219	Sony IMX708	Sony IMX708	Sony IMX477	Sony IMX296
Sensor resolution	2592 × 1944 pixels	3280 × 2464 pixels	4608 x 2592 pixels	4608 x 2592 pixels	4056 x 3040 pixels	1456 x 1088 pixels
Sensor image area	3.76 × 2.74 mm	3.68 x 2.76 mm (4.6 mm diagonal)	6.45 x 3.63mm (7.4mm diagonal)	6.45 x 3.63mm (7.4mm diagonal)	6.287mm x 4.712 mm (7.9mm diagonal)	6.3mm diagonal
Pixel size	1.4 μm × 1.4 μm	1.12 μm x 1.12 μm	1.4 μm x 1.4 μm	1.4 μm x 1.4 μm	1.55 µm x 1.55 µm	3.45 µm x 3.45 µm

Low Cost Camera - Raspberry Pi



Sony's Latest Sensor



Intelligent vision sensor stacked configuration

<Main functions on the logic chip>

Conventional image sensor operation circuit

- ISP which processes the image signal
- Original DSP dedicated to AI signal processing
- Memory for the AI model

⇒ Eliminates the need for high-performance processor or external memory

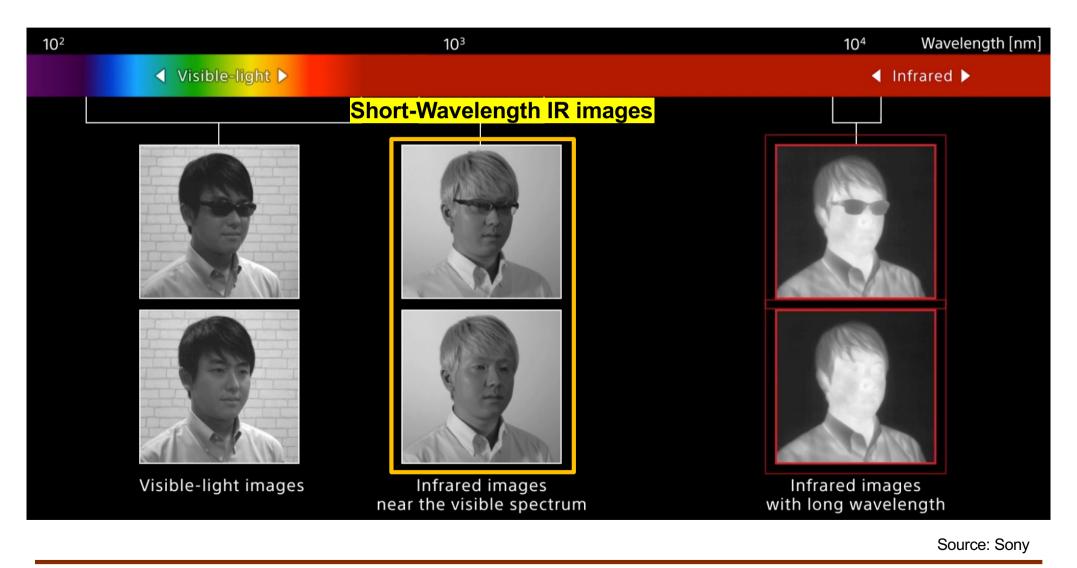
Source: Sony

Integration of AI into an Image Sensor



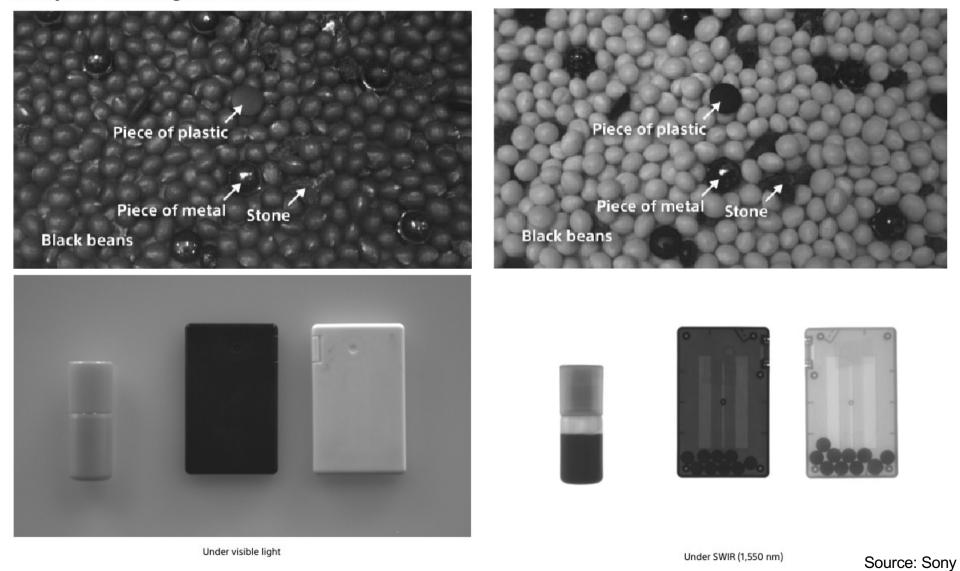
Source: Sony

Infrared (IR) and SWIR Images

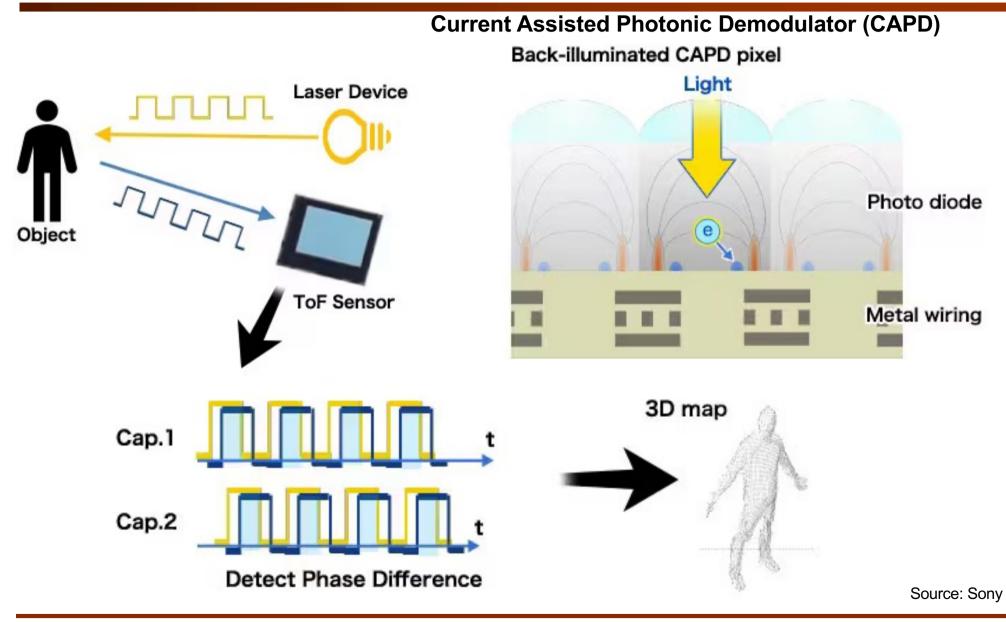


Infrared (IR) and SWIR Images

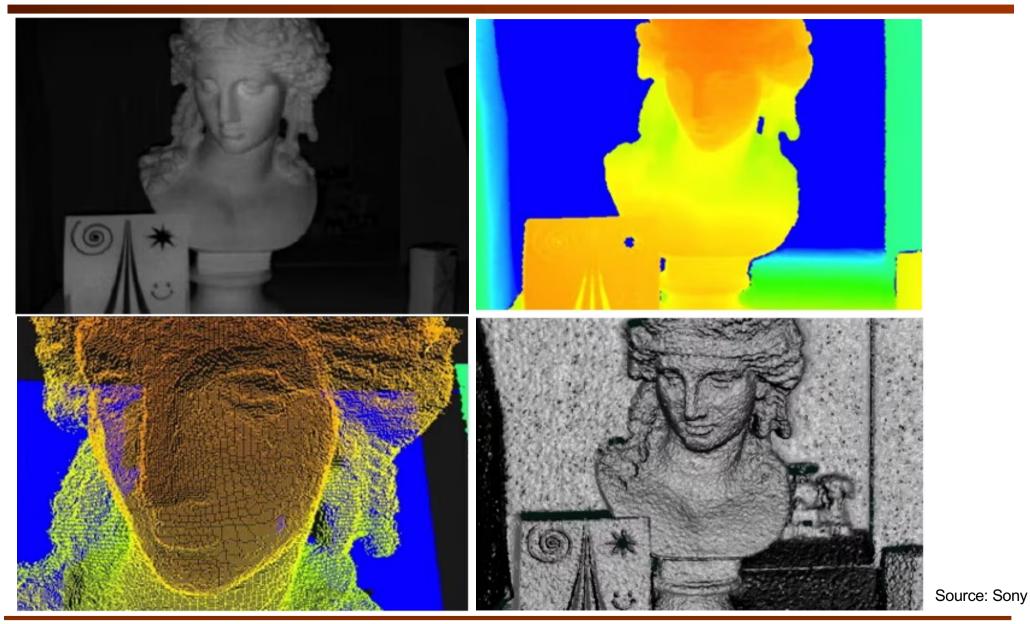
Example of detecting contaminants in food



Time of Flight (ToF) Image Sensor

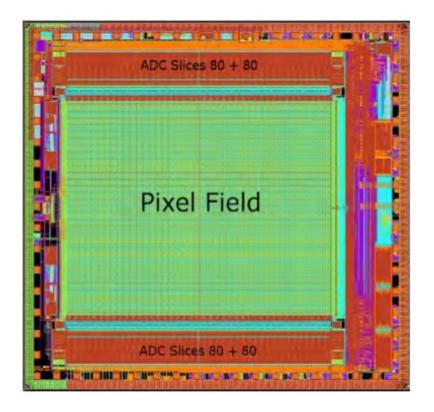


Time of Flight (ToF) Image Sensor



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Another ToF Sensor – epc660



epc660

3D TOF imager 320 x 240 pixel

Main Features

General

- □ 3D TOF imager in full monolithic design
- □ 320 x 240 pixel-field, backside illuminated
- □ QE >80% @ 850nm
- □ Full well capacity 8'000 ke- (ambient and signal)
- $\hfill \ensuremath{\square}$ 39 fps full 3D TOF frame rate, single frame rate up to 158 fps
- Region of interest setting allows up to several kfps
- □ 4 integrated temperature sensors

Measurement performance

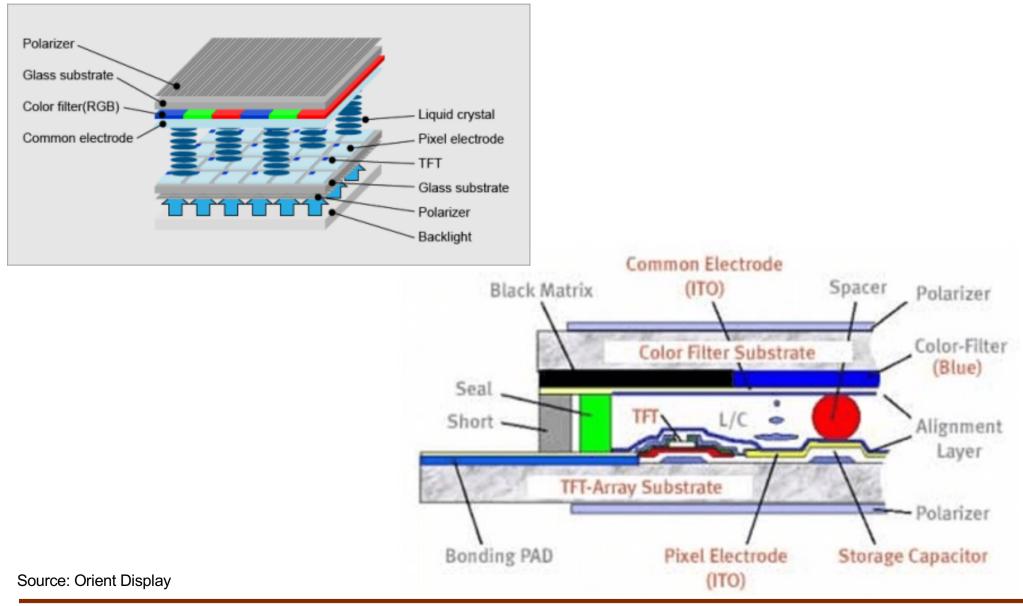
 Absolute accuracy in the sub-centimeter range with appropriate setup and calibration

Integrated LED (or laser diode) driver

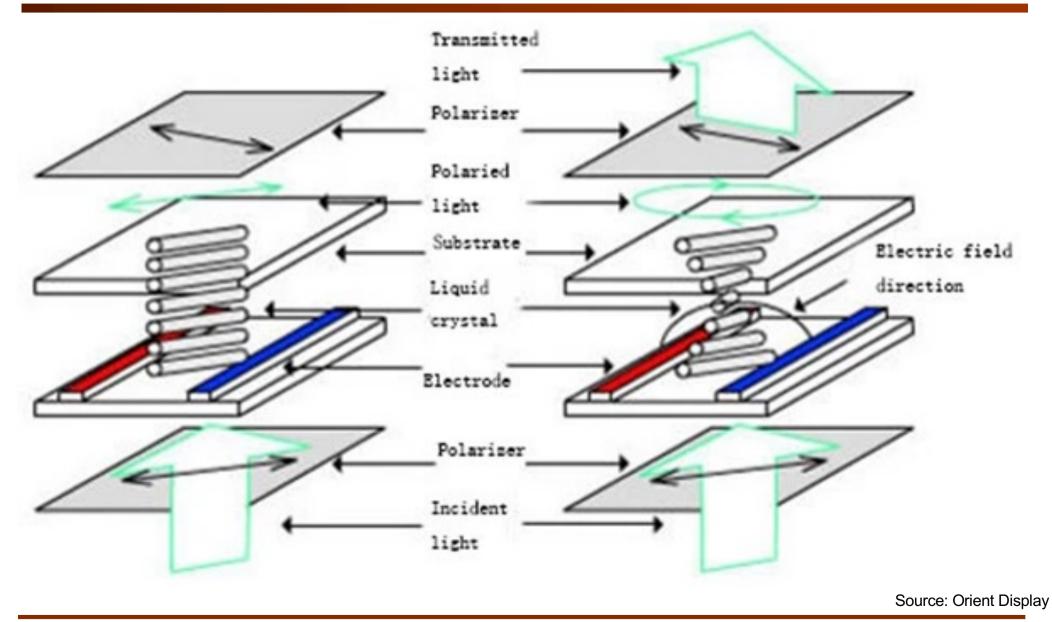
- Laser diode (LD) illumination possible
- □ Open-drain LED output pad, up to 200mA drive
- □ Push-pull LED2 output pad, up to 50mA drive
- Parallel digital data interface TCMI
 - □ 48MS/s max. data rate, 2.5/3.3V compatible
 - 12/8-bit parallel DATA output + XSYNC/SAT flag
 - USYNC, HSYNC and DCLK outputs
- I²C control interface (slave) 400kHz (FM) / 1MHz (FM+)
- Integrated EEPROM 128 x 8-bit
 - □ Calibration data and user programmable parameters
 - Unique chip ID

Source: EPC

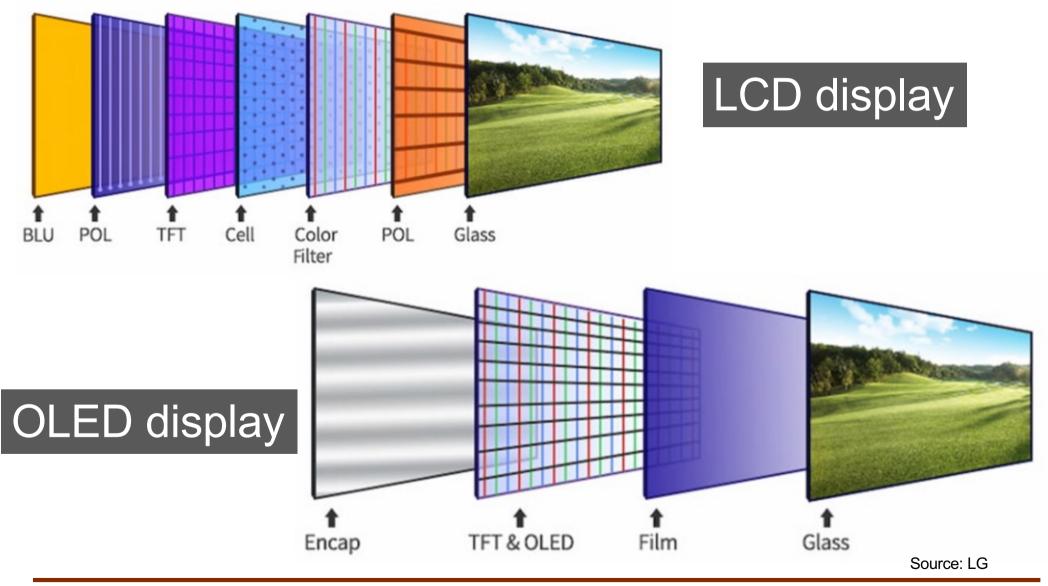
TFT LCD Technology



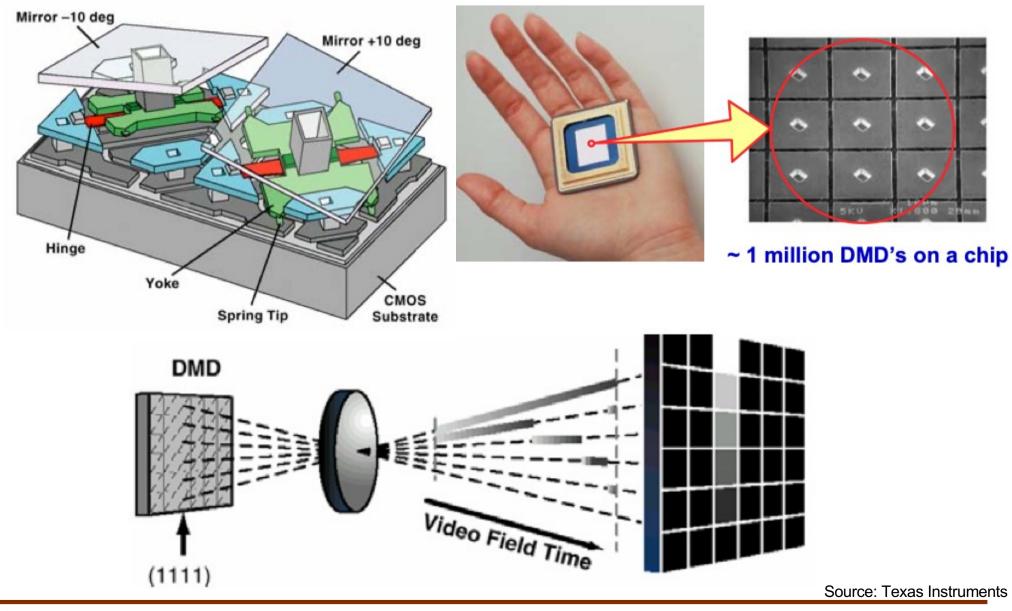
In-plane-switching (IPS) LCD Technology



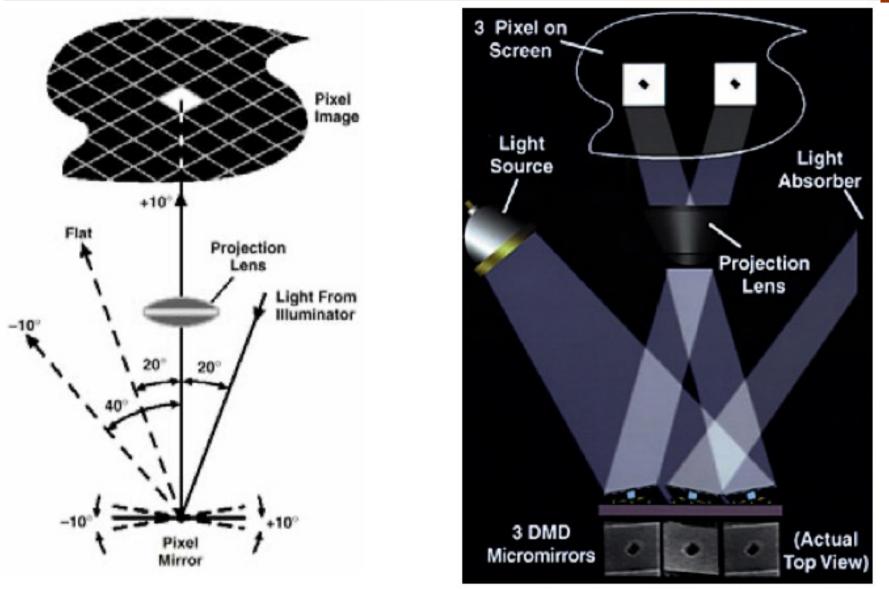
OLED Display Technology



Digital Micromirror Device (DMD) Technology

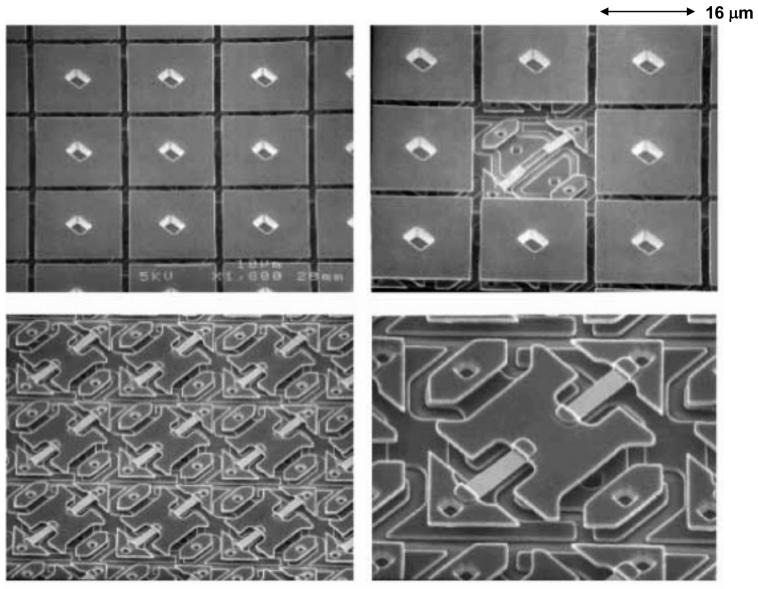


Principle of Projection using DMD



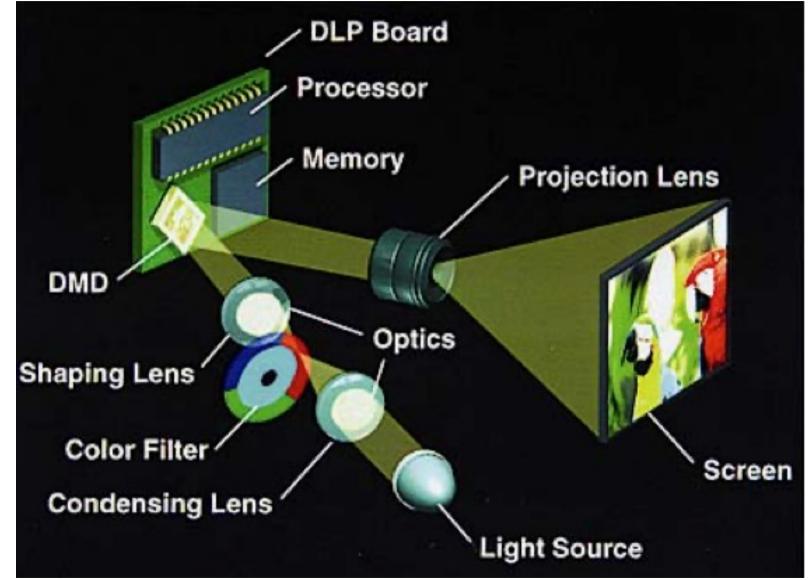
Source: Texas Instruments

SEM images of DMD by TI



Source: Texas Instruments

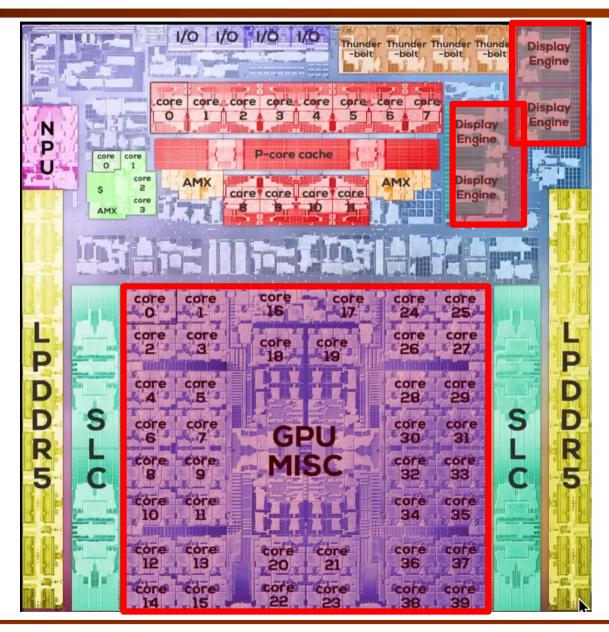
Digital Micromirror Device (DMD) Technology



DLP – Digital Light Processing

Source: Texas Instruments

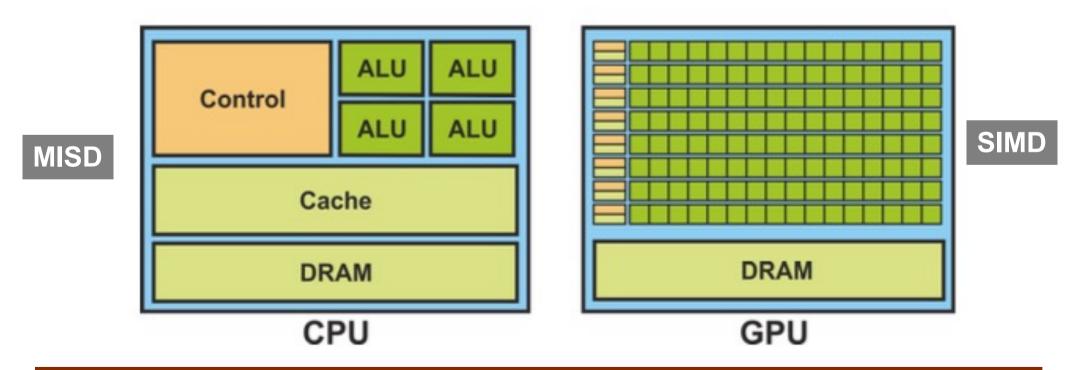
Apple Silicon M3 Pro Chip Photo



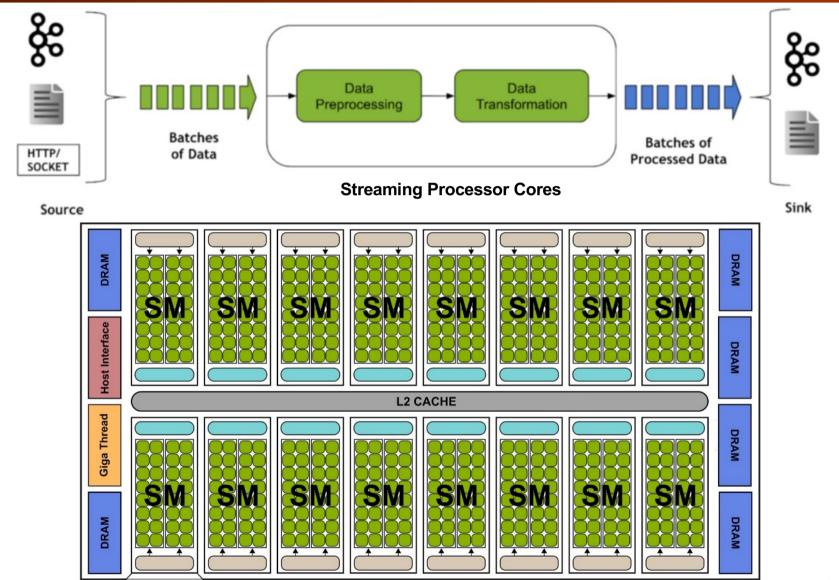
Source: Apple Computers

What is a GPU?

- Based on SIMD architecture Single Instruction, Multiple Data.
- Exploit data parallelism.
- High compute density due to massive degree of parallel processing.
- Initially developed as graphics accelerators for games.
- Now used for many other scientific processing and particularly for AI training.
- Software based on C/C++, and also on CUDA (Nvidia's own programming language).

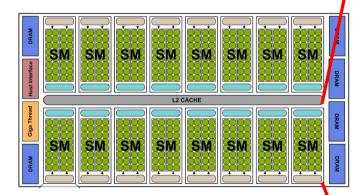


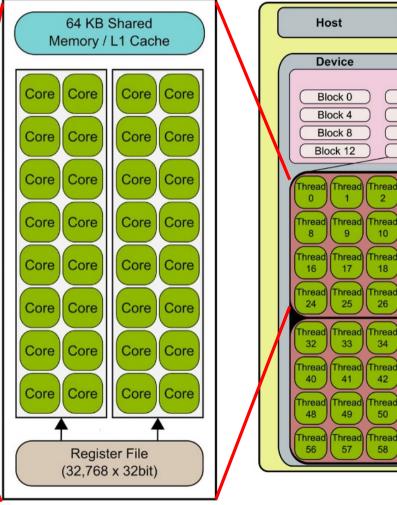
Typical Nvidia GPU Architecture



Source: NVIDIA

SM and the CUDA programming model

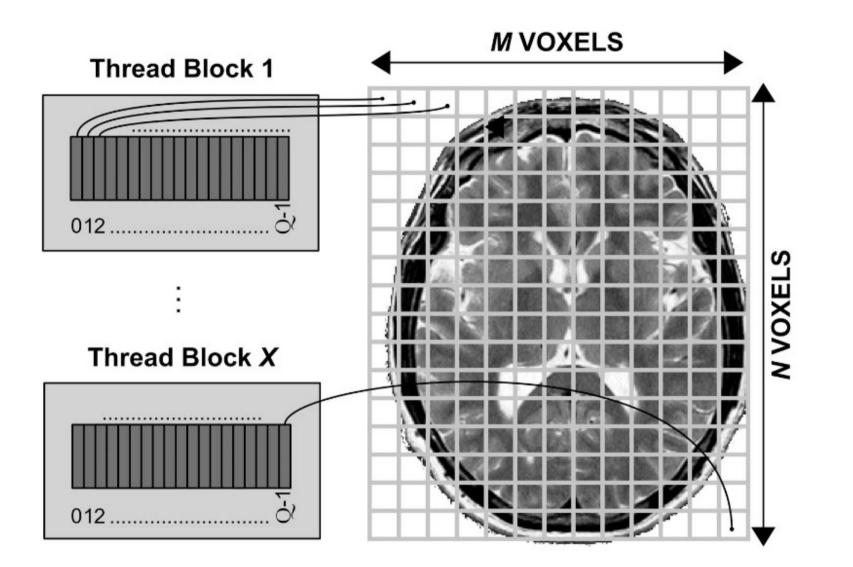




Kernel 0 Grid 0 Block 1 Block 2 Block 3 Block 5 Block 6 Block 7 Block 9 Block 10 Block 11 Block 13 Block 14 Block 15 hread (Thread) (Thread) (Thread) (Thread) Thread (Thread) (Thread) Block 13 5 (Thread) (Thread) (Thread) (Thread) Thread (Thread) (Thread 13 11 12 14 15 Warp 0 (Thread) Thread (Thread Thread (Thread) Thread 19 20 21 22 23 Thread Thread Thread Thread (Thread) Thread 27 28 29 30 31 (Thread) (Thread) (Thread) (Thread) Thread (Thread) (Thread Block 13 35 36 37 38 39 Thread Thread Thread Thread (Thread) (Thread 43 44 45 46 47 Warp 1 (Thread) (Thread) (Thread) (Thread) Thread (Thread) (Thread 51 52 53 54 55 Thread (Thread) (Thread) (Thread) Thread) (Thread) Thread 59 60 61 62 63

Source: NVIDIA

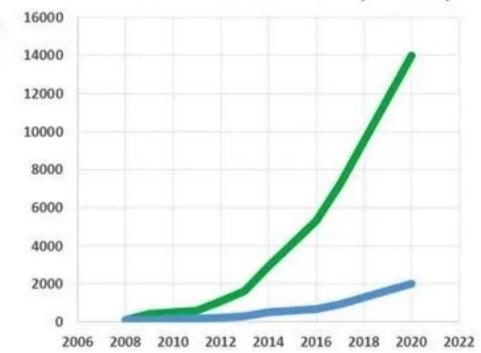
Nvidia CUDA Programming Model



Source: Moises Hernandez

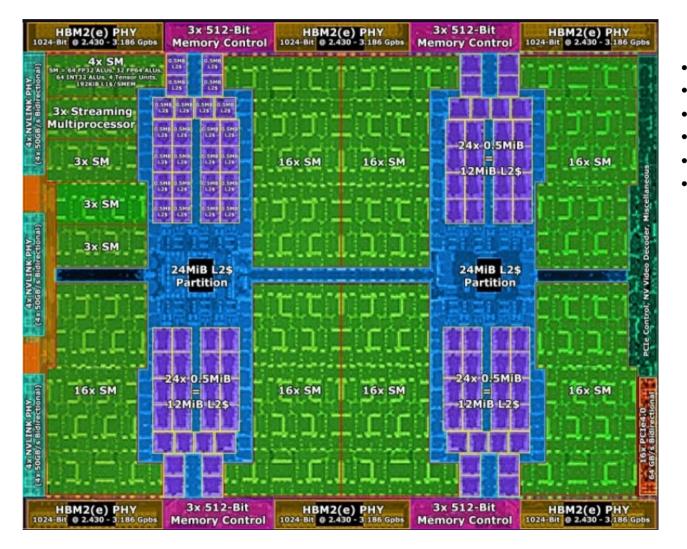
GPU vs CPU on Performance

Peak Memory Bandwidth (GB/s) GPU CPU



Peak Double Precision (GFLOPs)

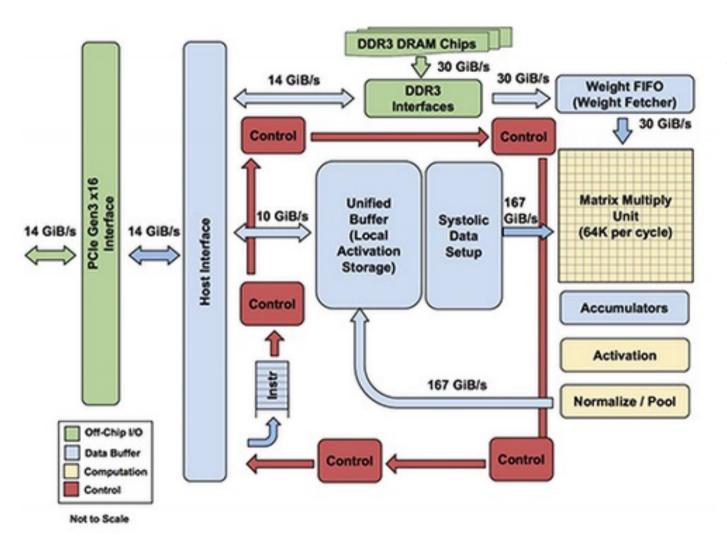
Nvidia Latest – Ada GPU AD102



- 288 FP64 cores in
- 144 Streaming Multiprocessors (SMs)
- 12 Graphics Processing Clusters (GPCs)
- 72 Texture Processing Clusters (TPCs)
- 384-bit memory interface
- 12 32-bit memory controllers.

Source: NVIDIA

Google Tensor Processing Unit (TPU)

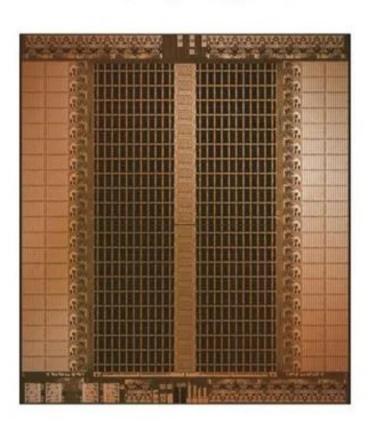


The TPU includes :

- Matrix Multiplier Unit (MXU): 65,536 8-bit multiply-and-add units for matrix operations
- **Unified Buffer (**UB): 24MB of SRAM that work as registers
- Activation Unit (AU): Hardwired activation functions

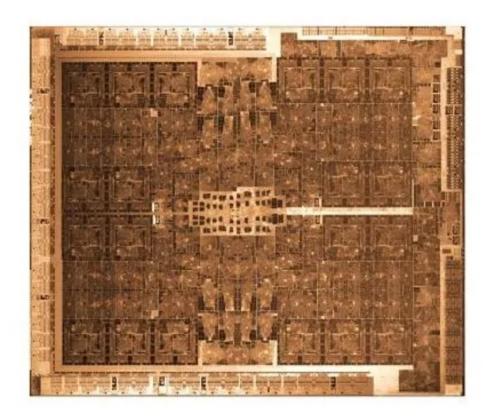
Source: Google

GroqChip 1 – Another AI inference engine



GroqChip[™] 1

Typical GPU —



Simplified design enables compute performance

Complex design for processing data results in **compute costs**

Source: Groq

Cerebras 1.2 trillion transistor AI interference engine

